

Figure 1

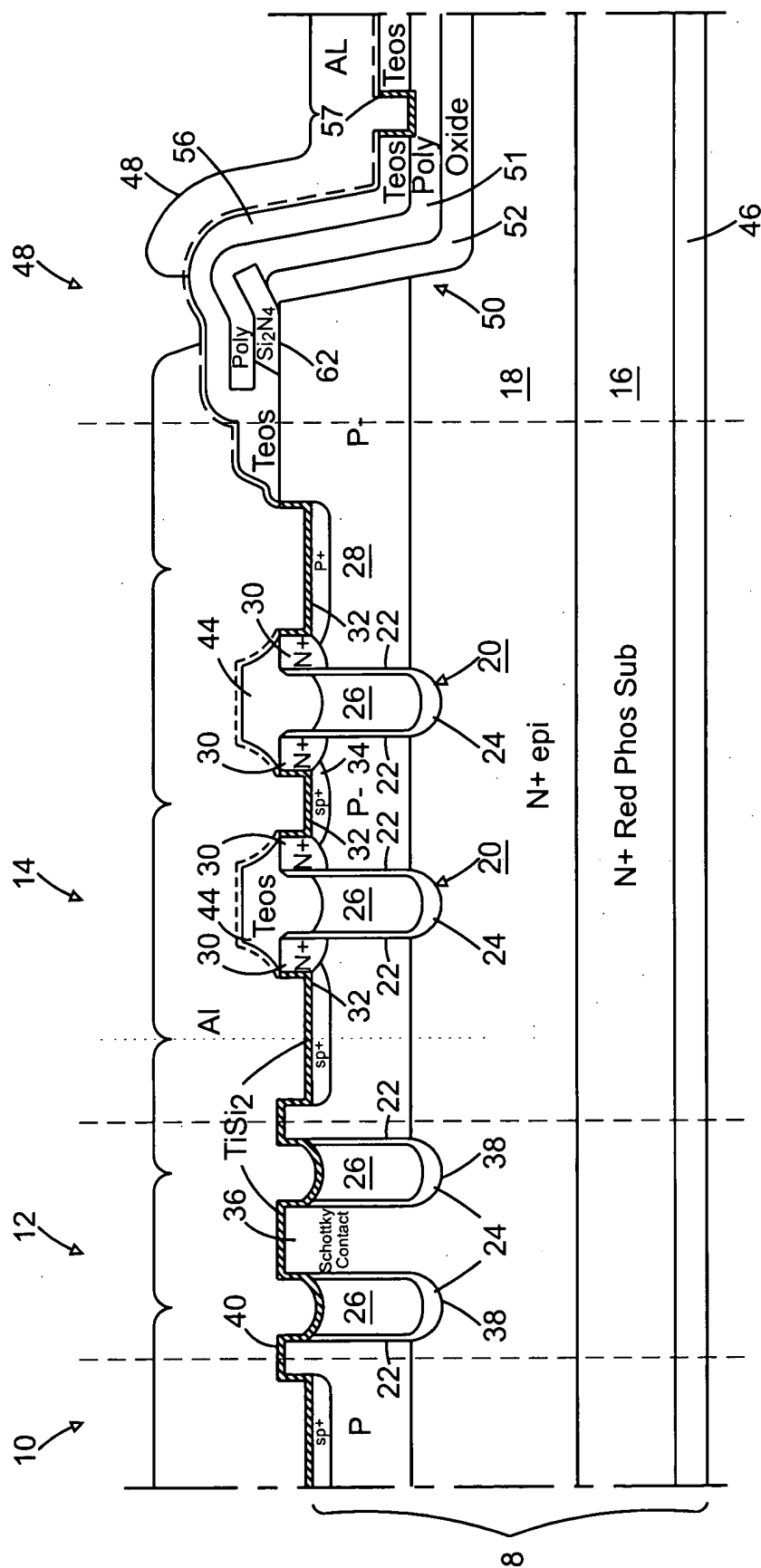


Figure 2



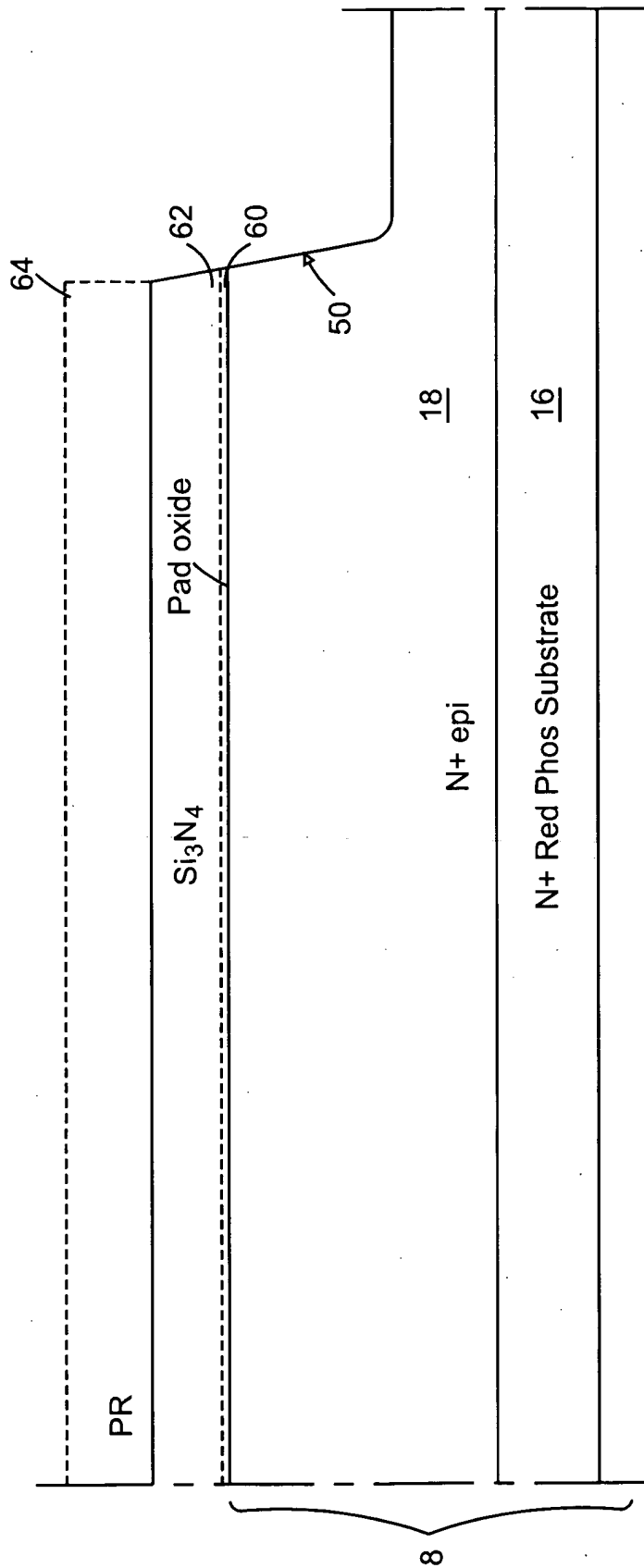


Figure 3



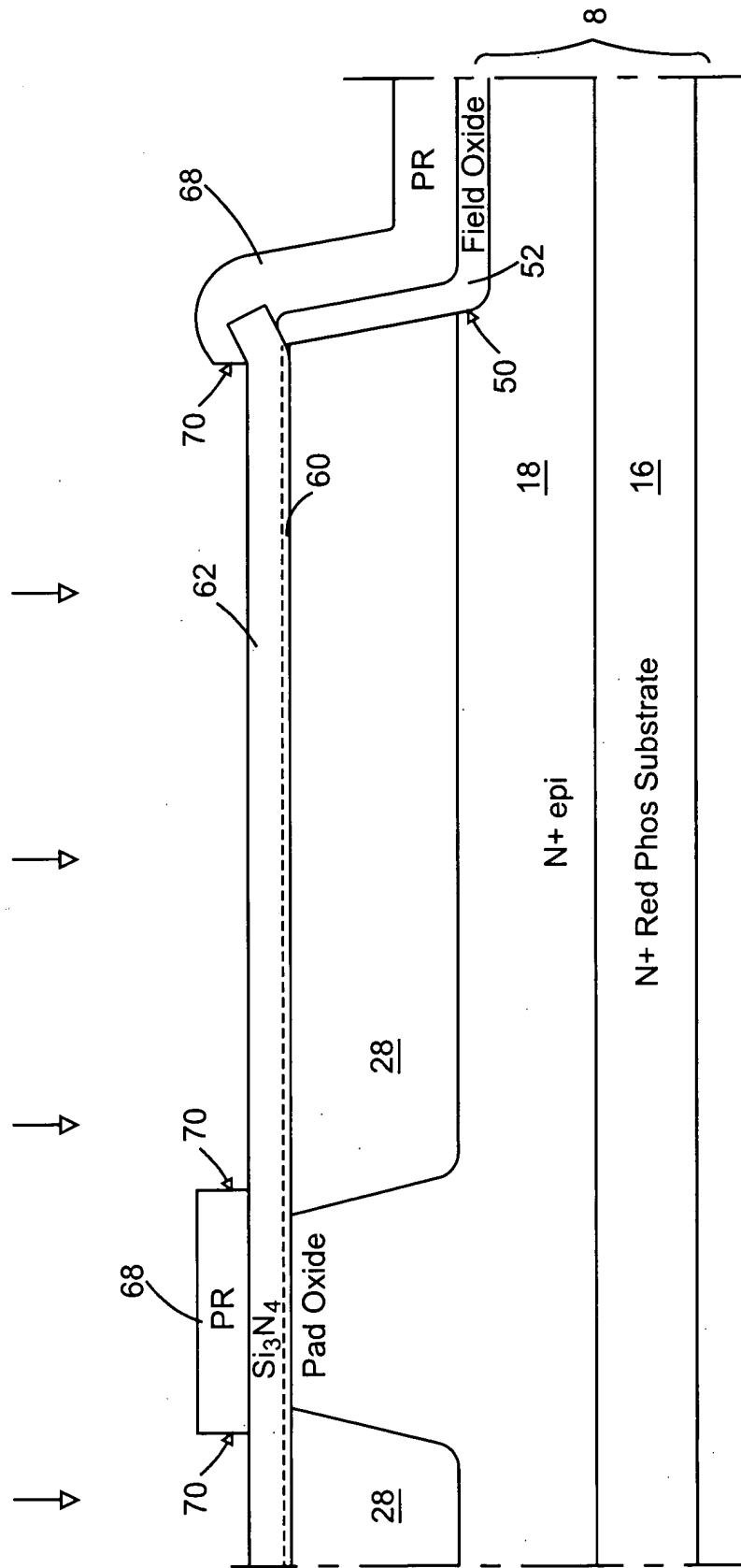


Figure 4



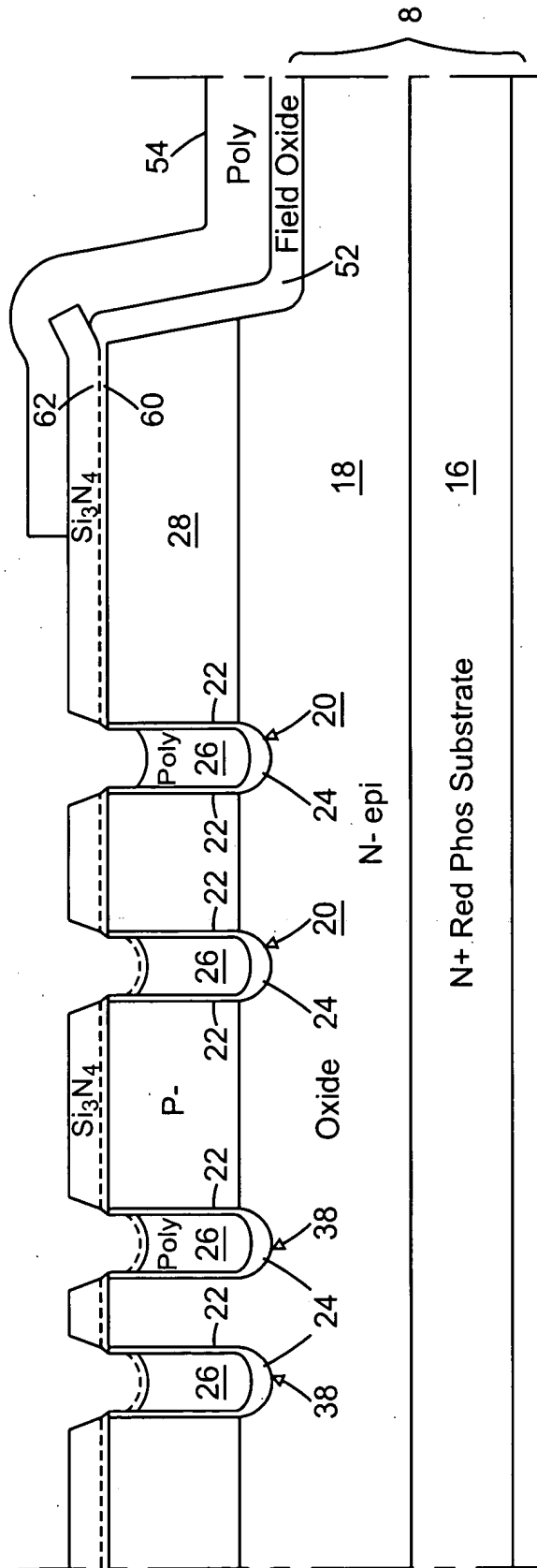


Figure 5



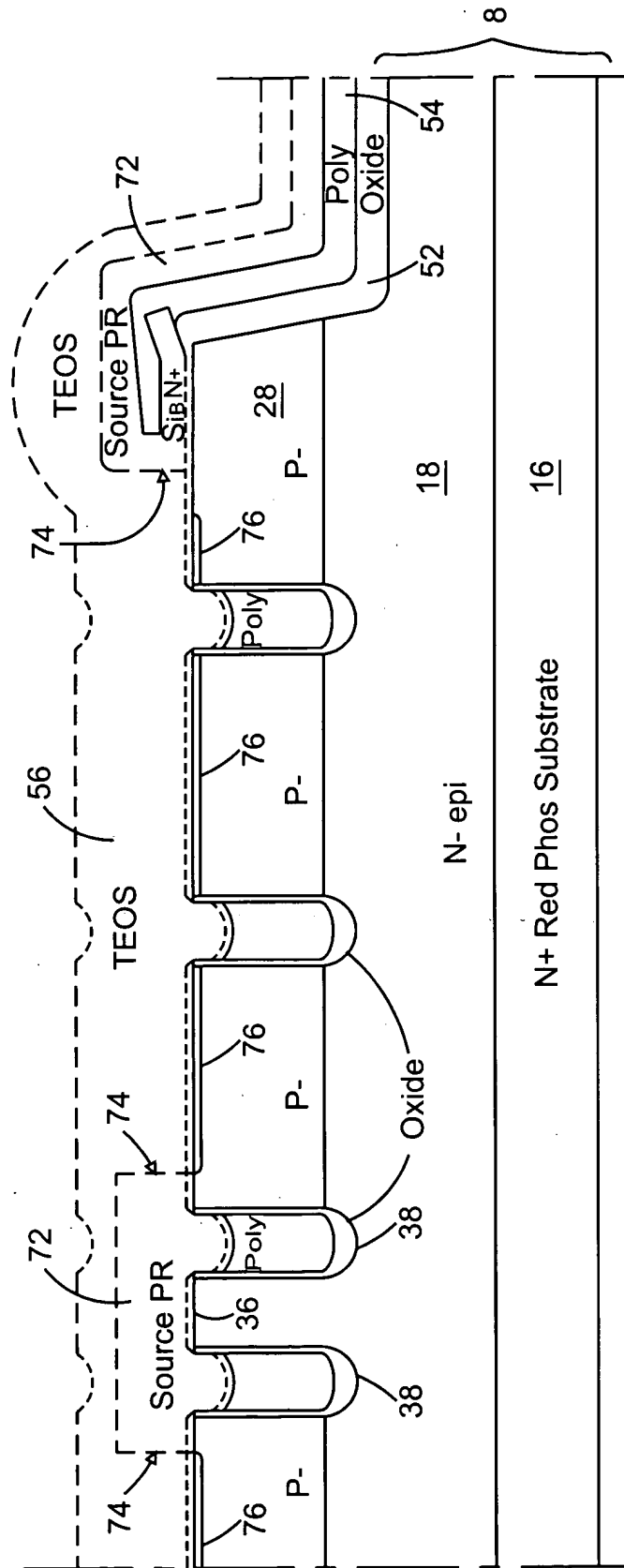


Figure 6



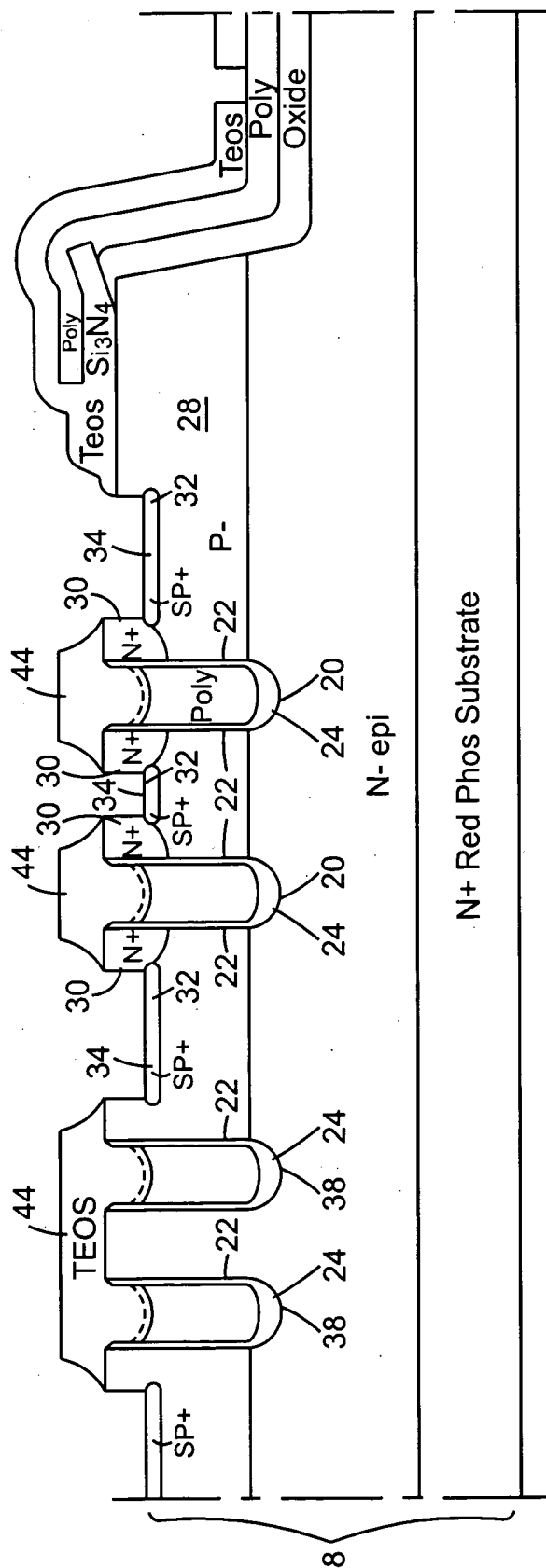


Figure 7



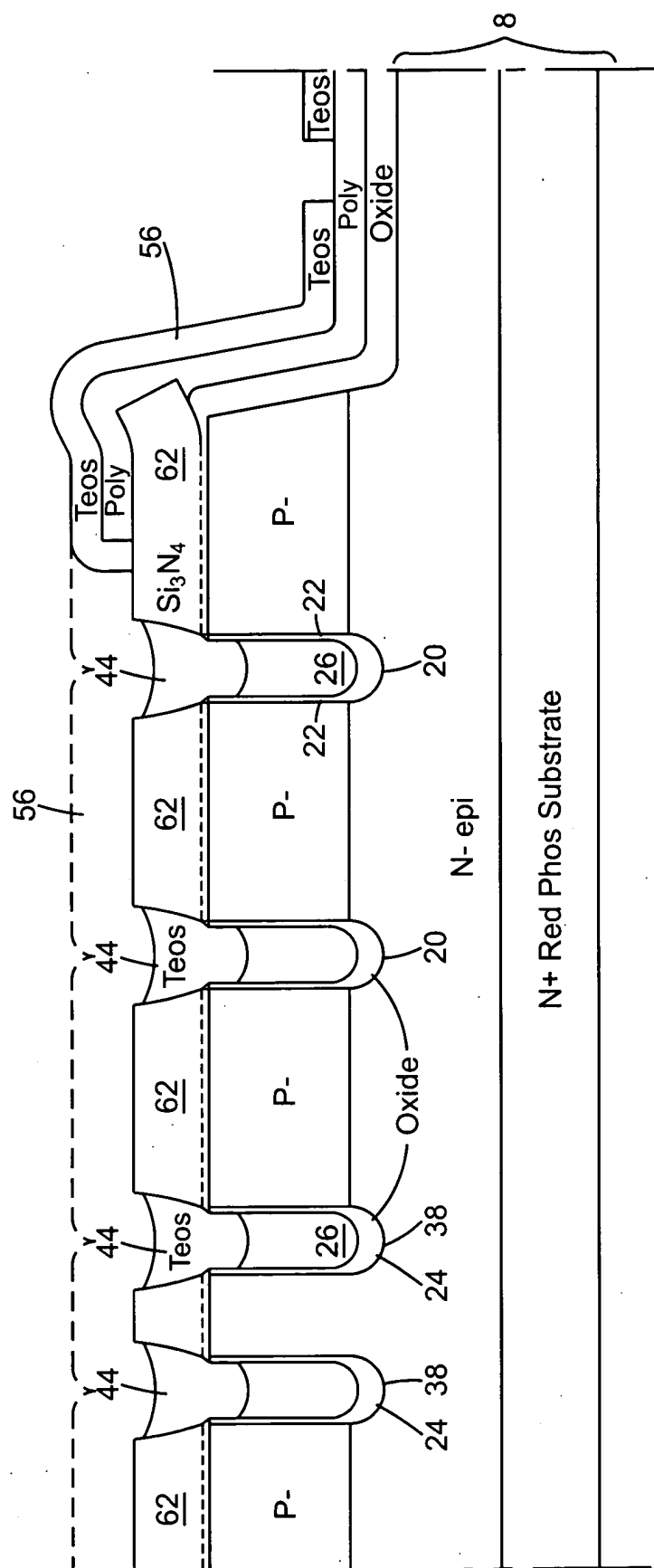


Figure 9



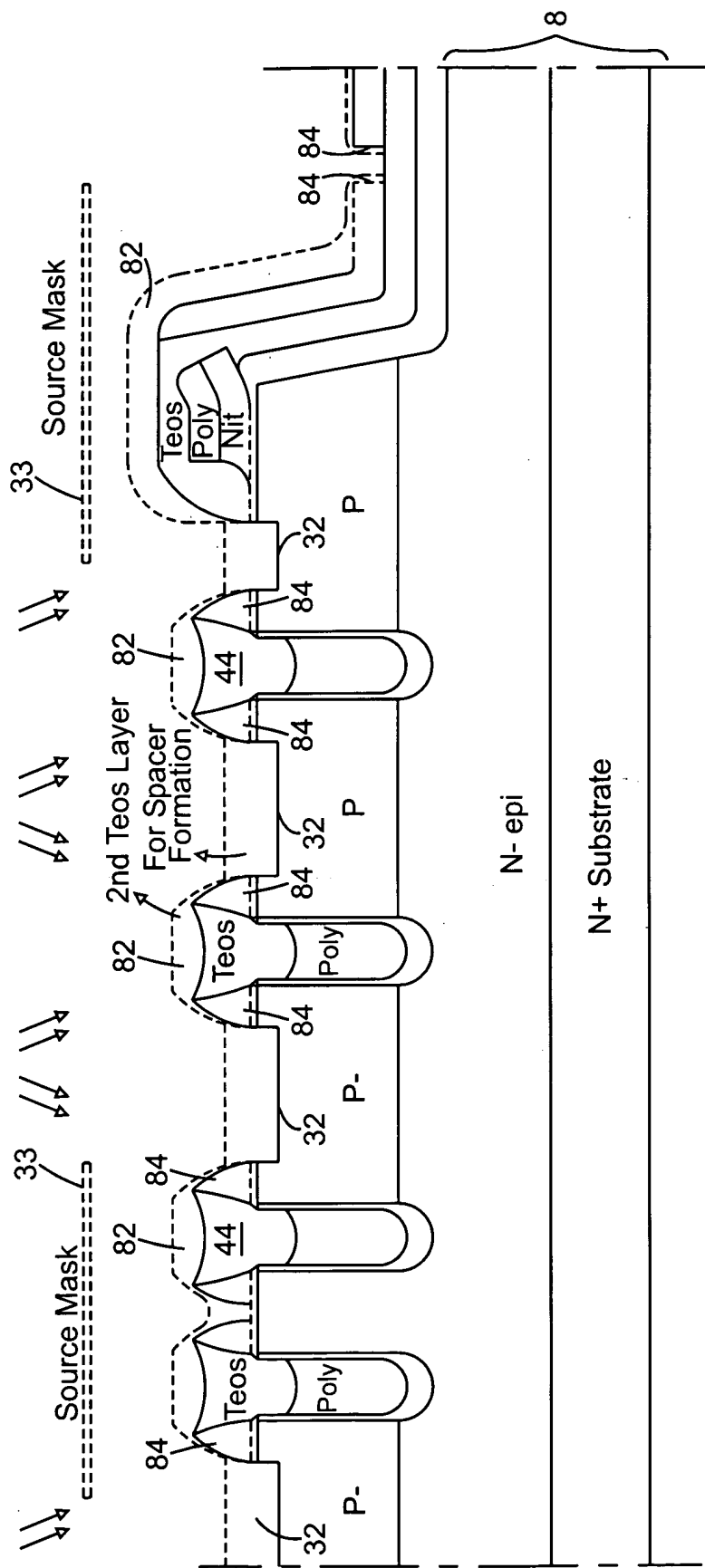


Figure 10



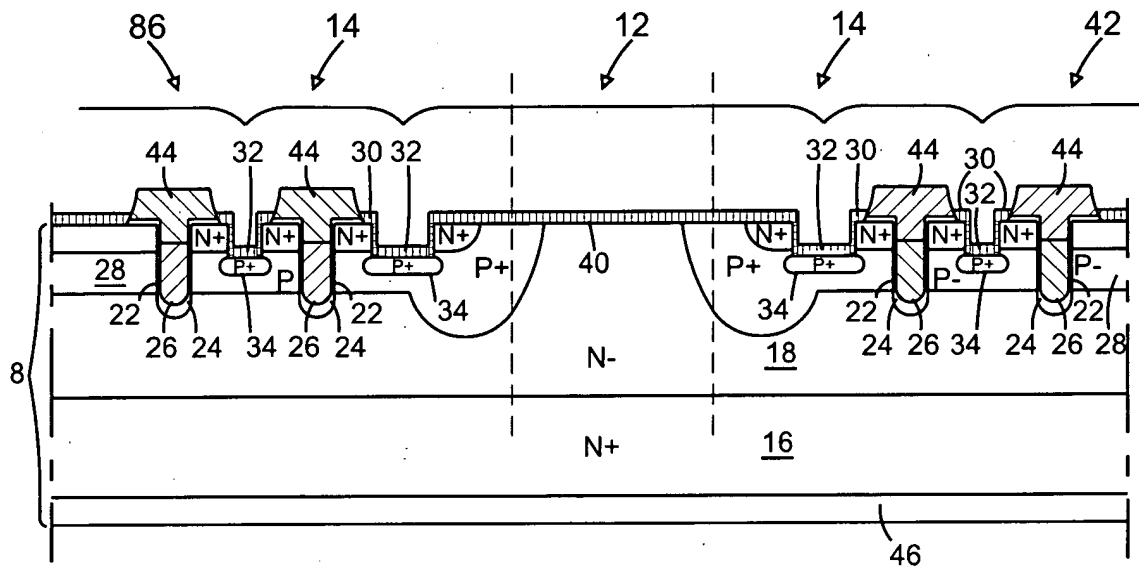
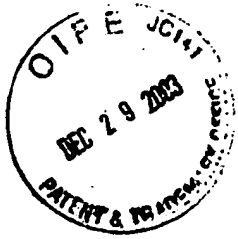


Figure 11

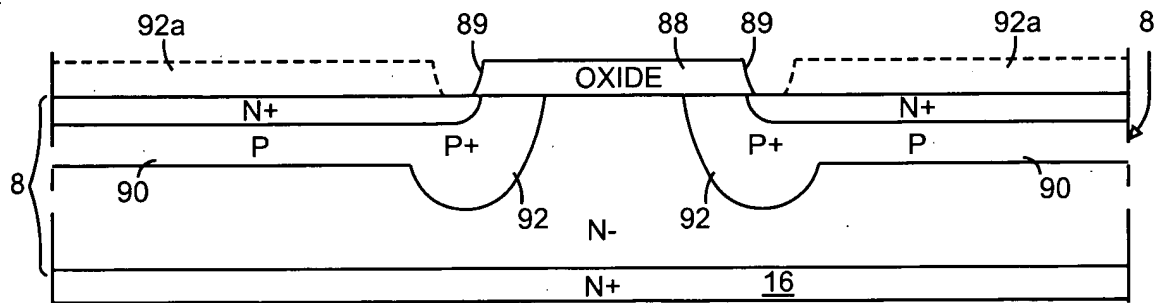
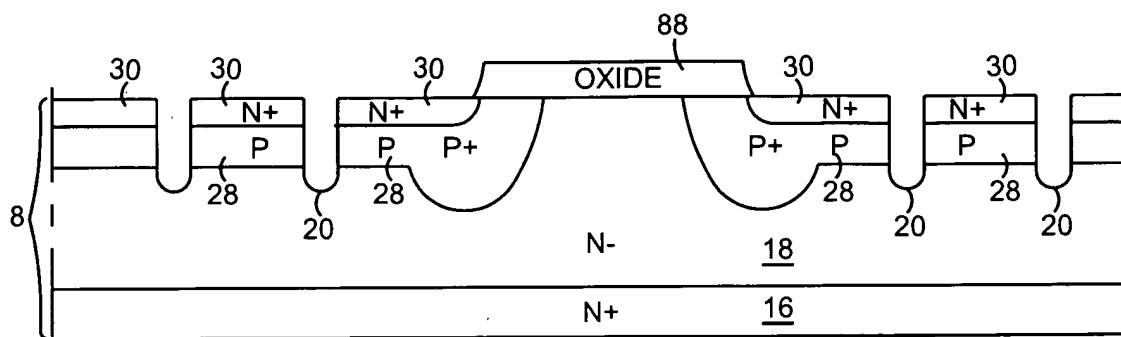


Figure 12



A cross-sectional view of a semiconductor device. The substrate consists of an N+ layer (16) and an N- layer (18). A P+ region (28) is formed in the N+ layer. A gate structure is formed on top of the substrate, consisting of an oxide layer (88) and N+ regions (30). The gate structure is divided into three sections by two vertical lines (26). The central section of the gate structure is labeled "OXIDE" and has a width of 88. The two side sections are labeled "N+" and have a width of 30. The substrate is labeled with "94" at the top and "20" at the bottom. The P+ region is labeled "28".

A cross-sectional view of a semiconductor device. The substrate consists of an N- region (labeled 18) and an N+ region (labeled 16). A gate stack is formed on the N- region, comprising an oxide layer (labeled 8) and a poly layer (labeled 18). The gate stack is divided into sections by spacers (labeled 32). The spacers are formed on the N+ region (labeled 16) and the N- region (labeled 18). The spacers are labeled 34. The gate stack is labeled 44. The oxide layer is labeled 96. The poly layer is labeled 98. The N+ region is labeled 96. The N- region is labeled 98. The substrate is labeled 8. The gate stack is labeled 16. The oxide layer is labeled 18. The poly layer is labeled 32. The spacers are labeled 34. The gate stack is labeled 44. The oxide layer is labeled 96. The poly layer is labeled 98. The N+ region is labeled 96. The N- region is labeled 98.

Figure 15